IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	ANDREW W. KRONE ET AL.
Filed:	HEREWITH
For:	DIGITAL ISOLATION SYSTEM WITH ADC OFFSET CALIBRATION
Serial No.:	UNKNOWN
Group Art Unit:	UNKNOWN
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Signature: Mary Jones Date: 9-26-03

Commissioner For Patents
P. O. Box 1450
Alexandria, VA 22313

Dear Sir:

PRELIMINARY AMENDMENT

Please amend the application as follows.

In The Specification:

On the cover page, and again at page 1, please replace the title with the following title: **Digital Isolation System With ADC Offset Calibration**

On page 1, lines 6-19:

This application is a continuation of co-pending U.S. Serial No. 10/161,902, filed on June 4, 2002 which is incorporated herein by reference, and which is a division of co-pending U.S.

Serial No. 09/035,180, filed on March 4, 1998, now U.S. Patent No. 6,442,213, which is ~~This is~~ a continuation-in-part of U. S. Serial Nos. 08/841,409, now U.S. Patent No. 6,137,827, 08/837,702, now U.S. Patent No. 5,870,046 and 08/837,714, now U.S. Patent No. 6,430,229 all filed on April 22, 1997. Further, the following U. S. patent applications ~~filed concurrently herewith~~ Serial No. 09/034,687, now U.S. Patent No. 6,359,983 [[_____]], entitled "Digital Isolation System With Data Scrambling" by ~~George Tyson Tuttle~~ Andrew W. Krone et al.; Serial No. 09/034,455, now U.S. Patent No. 6,480,602 [[_____]], entitled "Ring-Detect Interface Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. 09/035,779, now U.S. Patent No. 6,389,134 [[_____]], entitled "Call Progress Monitor Circuitry and Method for a Communication System" by Timothy J. Dupuis et al.; Serial No. 09/034,683, now U.S. Patent No. 6,167,134 [[_____]], entitled "External Resistor and Method to Minimize Power Dissipation in DC Holding Circuitry for a Communication System" by Jeffrey W. Scott et al.; Serial No. 09/034,620, now U.S. Patent No. 6,160,885 [[_____]], entitled "Caller ID Circuit Powered Through Hookswitch Devices" by Jeffrey W. Scott et al; Serial No. 09/034,682, now U.S. Patent No. 6,408,034 [[_____]], entitled "Framed Delta Sigma Data With Unlikely Delta Sigma Data Patterns" by Andrew W. Krone et al.; and Serial No. 09/035,175, now U.S. Patent No. 6,385,235 [[_____]], entitled "Direct Digital Access Arrangement Circuitry and Method for Connecting to Phone Lines" Jeffrey W. Scott et al., are expressly incorporated herein by reference.

On page 27, line 18 through page 28, line 6:

A preferred embodiment of frequency detector 818 is shown in Figure 10. The inputs to frequency detector 818 are the DATA and CK4 signals and the outputs are the SPEED-UP2 and SLOW-DOWN2 signals. Delay cell 880 has its input connected to CK4 and output connected to one input of NOR gate 882. The delay cell 880 consists of an even number of capacitively loaded inverter stages or other delay generating circuitry and is well known in the art. The output of inverter 884 is connected to the other input of NOR gate 882 and the input of inverter 884 is connected to CK4. The output 886 of NOR gate 882 is reset pulse that occurs on the rising edge of CK4, and is connected to the reset input of D flip-flops 888, 890, and 892. The input of inverter ~~894~~ 895 is connected to DATA. The output of inverter ~~894~~ 895 is connected to

the clock input of D flip-flops 888, 890, and 892. The D input of flip-flop 888 is connected to V_{DD}. The D-input of flip-flop 890 is connected to the Q-output of flip-flop 888. The D-input of flip-flop 892 is connected to the Q-output of flip-flop 890. D flip-flops 894 and 896 have their clock inputs connected to CK4. The D input of flip-flop 894 is connected to the Q output of flip-flop 888. The D-input of flip-flop 896 is connected to the Q-output of flip-flop 890. The input of inverter 898 is connected to the Q-output of flip-flop 894, and the output of inverter 898 is the SLOW-DOWN2 signal. OR gate 900 provides the SPEED-UP2 signal. One input of OR gate 900 is connected to the Q-output of flip-flop 896, and the other input is connected to the Q-output of flip-flop 892. The SPEED-UP2 and SLOW-DOWN2 signals are connected to the frequency-detector charge pump 824.

On page 30, lines 11-25:

The difference between the signals present at nodes A and B is provided by analog adder 142 to provide a base input signal on line 144. Selected bias levels may be applied to the ADC's and DAC's in this system in order to ensure good tone performance. At adder 150, a selected fixed ADC bias offset voltage provided by analog ADC bias source 146 is then added to the base input signal, as is an optional ~~course~~ coarse adjust offset voltage provided by coarse adjust digital-to-analog converter 148, which will be discussed further below. The output of adder 150 is provided as the input signal to delta-sigma analog-to-digital converter (ADC)152, which provides an oversampled 1-bit digital output signal to transmitter circuit 154 that transmits the signal across isolation barrier 132 to receiver circuit 156. The 1-bit digital signal is then combined with the inverse of the fixed ADC bias offset, provided by digital ADC bias source 159, in digital adder 158, which removes the fixed bias voltage from source 146 that was introduced through adder 150. The fixed bias voltage from source 146 is selected to optimize the operation of delta-sigma ADC 152 by causing it to operate in a preferred part of its range. The output of adder 158 provides a digital output signal corresponding to the incoming analog signal on line 144 which is provided to additional processing circuitry (not shown) through node C 138.

On page 32, line 24 through page 33, line 6:

In a preferred embodiment, calibration control logic 184 senses if the input to delta-sigma modulator 162 is outside of the desired range during the calibration cycle. If it is, control logic 184 provides an "up" or "down" control signal that is transmitted across isolation barrier 132 through transmitter 164 and receiver 166 and then routed to coarse offset DAC 148. Coarse ~~Course~~ offset DAC 148 is adapted to receive the "up" and "down" signals and to increment or decrement its output voltage in response thereto. Coarse offset DAC 148 may be designed to provide a variety of output voltage levels, which may be multiples of the preselected threshold value *delta* mentioned above. In preferred embodiments, coarse offset DAC 148 includes a coarse offset register that holds a digital value that is converted to an output voltage by the DAC. The least significant bit of that register is chosen to represent an output voltage change of less than two times *delta*. When "up" and "down" signals are received by coarse offset DAC 148, they cause the value in the coarse offset register to increment or decrement by "1", respectively, resulting in a step-wise change in the coarse offset voltage signal.

On page 33, lines 7-17:

After the coarse offset voltage is added to the loop at adder 150, the calibration operation continues as the integrator monitors the signal at node C and provides an output variable offset signal. If control logic 184 again detects that the input to delta-sigma modulator 162 is outside of the desired range, another up or down signal may be sent to cause coarse offset DAC 148 to add another unit of ~~course~~ coarse offset voltage through adder 150. Eventually the calibration loop will stabilize with a signal corresponding to zero volts at node C, with a calibrated offset voltage provided by the combination of coarse offset DAC 148 and register 182, both of which are held constant during normal operation of the isolation barrier system. In preferred embodiments, coarse offset modifications are only made in the first half of the On page 1, lines 6-19: